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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,871	03/22/2004	Robert Tod Dimpsey	AUS920040064US1	2672

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EXAMINER	
SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,871	DIMPSEY ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☑ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed December 18, 2006 in response to the Office action dated September 18, 2006. Claim 18 has been amended. Claims 1-24 are pending in this application.

OBJECTIONS

Specification

1. In the section entitled "Cross Reference to Related Applications" Applicant must properly identify all co-pending applications with their corresponding application numbers (i.e. serial numbers).

2. In view of Applicant's amendment, the objection to the title has been withdrawn.

REJECTIONS NOT BASED ON PRIOR ART

Double Patenting

3. In view of Applicant's terminal disclaimer filed with the amendment, the provisional double-patenting rejections to **claims 1, 3-6, 8, 11, 13-15, 18, and 20-22** have been withdrawn.

Claim Rejections - 35 USC § 101

4. In view of Applicant's amendment, the 101 rejections to **claims 18-24** have been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-2, 5, 7-12, 15, 17-19, 22, and 24 are rejected under 35 U.S.C. 103(a) as being obvious over Matsubara (U.S. Patent 6,381,679) in view of Anonymously Disclosed, "Method for the dynamic prediction of nonsequential memory accesses", hereafter "Anon."

7. **As per claims 1 and 18**, Matsubara discloses a method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:

responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction (col. 5, lines 1-10; col. 6, lines 35-42 and 53-55; col. 7, lines 10-20; Fig. 1; Fig. 2, elements 21 and 22; Fig. 6B). *It should be noted that computer program product in claims 18-24 executes the exact same functions as the methods in claims 1-7. Therefore, any references that teach claims 1-7 also teach the corresponding claims 18-24. It should also be noted that the "indication bits (i.e. PF bits)" equaling 1 is analogous to the "prefetch indicator being associated with the instruction" and the "CPU 21" is analogous*

to the "processor unit." Lastly, it should be noted that the "instruction fetch (IF)" stage is when the instruction in the code is loaded into a cache and the "decoding" stage is when the "determination" is made.

and responsive to the prefetch indicator being associated with the instruction, selectively prefetching data into the cache in the processor (col. 6, lines 53-55; Fig. 2, elements 21 and 22). *It should be noted that when it is determined that the value of the PF bits is 1, all the data of the line is prefetched to the primary cache.*

Matsubara does not expressly disclose a pointer to a data structure identified by the prefetch indicator.

Anon discloses a pointer to a data structure identified by the prefetch indicator (General Description, 1st paragraph and 4th paragraph; Detailed Description, 1st paragraph). *It should be noted that the "dynamic prefetch pointer" is analogous to the "pointer to a data structure."*

Matsubara and Anon are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Anon's dynamic prefetch pointer within Matsubara's information processing system.

The motivation for doing so would have been to improve memory access due to improved memory access prediction and also improve performance due to reducing the time spent waiting for memory accesses to complete (Anon, General Description, 5th paragraph).

Therefore, it would have been obvious to combine Matsubara and Anon for the benefit of obtaining the invention as specified in claims 1 and 18.

8. **As per claims 2 and 19**, the combination of Matsubara/Anon discloses the prefetch indicator contains the pointer to the data structure (Anon, General Description, 4th paragraph).

9. **As per claims 5 and 22**, the combination of Matsubara/Anon discloses the processor unit is selected from one of an instruction cache, data cache, or a load/store unit (Matsubara, col. 6, lines 35-42; col. 7, lines 10-20; Fig. 2, element 21). *It should be noted that the "CPU 21" is analogous to a "load/store unit."*

10. **As per claims 7 and 24**, the combination of Matsubara/Anon discloses the cache is a data cache (Matsubara, col. 8, lines 56-63).

11. **As per claim 8**, Matsubara discloses a data processing system comprising:

a cache in a processor in the data processing system (Fig. 2, elements 21 and 22);

and a load/store unit in the processor, wherein the load/store unit determines whether a prefetch indicator is associated with an instruction in response to loading the instruction for execution into the cache, the load/store unit selectively prefetches data into the cache using metadata associated with the instruction (col. 5, lines 1-10; col. 6, lines 35-42 and 53-55; col. 7, lines 10-20; Fig. 1; Fig. 2, elements 21 and 22; Fig. 6B). *It should be noted that the "indication bits (i.e. PF bits)" are analogous to the "prefetch indicator" as well as the "metadata." It should also be noted that when it is determined that the value of the PF bits is 1, all the data of the line is prefetched to the primary*

cache.

Matsubara does not expressly disclose a pointer to a data structure identified by the prefetch indicator.

Anon discloses a pointer to a data structure identified by the prefetch indicator (General Description, 1st paragraph and 4th paragraph; Detailed Description, 1st paragraph). *See the citation note for the similar limitation in claims 1 and 18 above.*

Matsubara and Anon are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Anon's dynamic prefetch pointer within Matsubara's information processing system.

The motivation for doing so would have been to improve memory access due to improved memory access prediction and also improve performance due to reducing the time spent waiting for memory accesses to complete (Anon, General Description, 5th paragraph).

Therefore, it would have been obvious to combine Matsubara and Anon for the benefit of obtaining the invention as specified in claim 8.

12. **As per claim 9**, the combination of Matsubara/Anon discloses the cache is at least one of an instruction cache and a data cache (Matsubara, col. 8, lines 56-63). *It should be noted that Matsubara discloses the cache is a data cache.*

13. **As per claim 10**, Matsubara discloses the load/store unit selectively prefetches data based on a determination by the cache as to whether the prefetch is to occur (col.

7, lines 18-32). *It should be noted that the prefetch occurs based on whether there is a "hit" or "miss" in the secondary cache.*

Matsubara does not expressly disclose a pointer to a data structure.

Anon discloses a pointer to a data structure (General Description, 1st paragraph; Detailed Description, 1st paragraph).

Please see the 103 rejection of claim 8 above for the reasons to combine Matsubara and Anon.

14. **As per claim 11**, Matsubara discloses a data processing system for providing hardware assistance to prefetch data during execution of code by a process or in the data processing system, the data processing system comprising:

determining means, responsive to loading an instruction in the code into a cache, for determining, by the a processor unit, whether a prefetch indicator is associated with the instruction (col. 5, lines 1-10; col. 6, lines 35-42 and 53-55; col. 7, lines 10-20; Fig. 1; Fig. 2, elements 21 and 22; Fig. 6B); *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 1 and 18 above.*

and selectively prefetching means, responsive to the prefetch indicator being associated with the instruction, for selectively prefetching data into the cache in the processor (col. 6, lines 53-55; Fig. 2, elements 21 and 22). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 1 and 18 above.*

Matsubara does not expressly disclose a pointer to a data structure identified by

the prefetch indicator.

Anon discloses a pointer to a data structure identified by the prefetch indicator (General Description, 1st paragraph and 4th paragraph; Detailed Description, 1st paragraph). *See the citation note for the similar limitation in claims 1 and 18 above.*

Matsubara and Anon are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Anon's dynamic prefetch pointer within Matsubara's information processing system.

The motivation for doing so would have been to improve memory access due to improved memory access prediction and also improve performance due to reducing the time spent waiting for memory accesses to complete (Anon, General Description, 5th paragraph).

Therefore, it would have been obvious to combine Matsubara and Anon for the benefit of obtaining the invention as specified in claim 11.

15. **As per claim 12**, the combination of Matsubara/Anon discloses the prefetch indicator contains the pointer to the data structure (Anon, General Description, 4th paragraph).

16. **As per claim 15**, the combination of Matsubara/Anon discloses the processor unit is selected from one of an instruction cache, data cache, or a load/store unit (Matsubara, col. 6, lines 35-42; col. 7, lines 10-20; Fig. 2, element 21). *See the citation note for claims 5 and 22 above.*

17. **As per claim 17**, the combination of Matsubara/Anon discloses the cache is a data cache (Matsubara, col. 8, lines 56-63).

18. Claims 3, 13, and 20 are rejected under 35 U.S.C. 103(a) as being obvious over Matsubara in view of Anon as applied to claims 1 and 11 above, and in further view of IBM Technical Disclosure, "Cache Miss Director – A Means of Prefetching Cache Missed Lines," hereafter "IBMTD."

19. **As per claims 3 and 20**, the combination of Matsubara/Anon discloses all the limitations of claims 3 and 20 except determining whether outstanding cache misses are present;

and prefetching the data if a number of outstanding cache misses are less than a threshold.

IBMTD discloses determining whether outstanding cache misses are present (Discourse Text, lines 13-14); *It should be noted that the "demand miss" is analogous to the "cache miss."*

and prefetching the data if a number of outstanding cache misses are less than a threshold (Discourse Text, lines 14-17). *It should be noted that this limitation contains language that suggests or makes optional but does not require steps to be performed or does not limit the claim to a particular structure and therefore does not limit the scope of a claim. The term 'if' denotes an optionally recited limitation and optionally recited limitations are not guaranteed to take place. Thus, simply "prefetching the data" is disclosed because the optionally recited parts of this limitation are not required to be taught by the Office. See MPEP §2106, Section II(C)). It should also be noted that*

"anticipatory cache misses" are analogous to "prefetching data."

The combination of Matsubara/Anon and IBMTD are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement IBMTD's Cache Miss Directory (CMD) within Matsubara/Anon's information processing system.

The motivation for doing so would have been to get the lines into the cache before a demand miss occurs for them, thus, reducing processing delays (IBMTD, Discourse Text, lines 2-3 and 19-20).

Therefore, it would have been obvious to combine Matsubara, Anon, and IBMTD for the benefit of obtaining the invention as specified in claims 3 and 20.

20. **As per claim 13**, the combination of Matsubara/Anon/IBMTD discloses means for determining whether outstanding cache misses are present (IBMTD, Discourse Text, lines 13-14); *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 3 and 20 above.*

and means for prefetching the data if a number of outstanding cache misses are less than a threshold (IBMTD, Discourse Text, lines 14-17). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 3 and 20 above.*

21. Claims 4, 6, 16, 21, and 23 are rejected under 35 U.S.C. 103(a) as being obvious over Matsubara in view of Anon as applied to claims 1 and 11 above, and

in further view of Malik (U.S. Patent 6,687,794).

22. **As per claims 4 and 21**, the combination of Matsubara/Anon discloses all the limitations of claims 4 and 21 except determining whether to replace cache lines;

and prefetching the data if a number of cache lines chosen to be replaced are greater than a threshold.

Malik discloses determining whether to replace cache lines (col. 4, lines 60-63);

and prefetching the data if a number of cache lines chosen to be replaced are greater than a threshold (col. 5, lines 16-19). *It should be noted that this limitation contains language that suggests or makes optional but does not require steps to be performed or does not limit the claim to a particular structure and therefore does not limit the scope of a claim. The term 'if' denotes an optionally recited limitation and optionally recited limitations are not guaranteed to take place. Thus, simply "prefetching the data" is disclosed because the optionally recited parts of this limitation are not required to be taught by the Office. See MPEP §2106, Section II(C)).*

The combination of Matsubara/Anon and Malik are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Malik's prediction history within Matsubara/Anon's information processing system.

The motivation for doing so would have been to provide a technique to increase the performance of the data cache by reducing the possibility if a data cache miss (Malik, col. 4, lines 53-55).

Therefore, it would have been obvious to combine Matsubara, Anon, and Malik for the benefit of obtaining the invention as specified in claims 4 and 21.

23. **As per claims 6 and 23**, the combination of Matsubara/Anon/Malik discloses the cache is an instruction cache (Malik, col. 4, lines 10-12; Fig. 3, elements 300 and 310).

24. **As per claim 14**, the combination of Matsubara/Anon/Malik discloses means for determining whether to replace cache lines (col. 4, lines 60-63); *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer.*

and means for prefetching the data if a number of cache lines chosen to be replaced are greater than a threshold (col. 5, lines 16-19). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 4 and 21 above.*

25. **As per claim 16**, the combination of Matsubara/Anon/Malik discloses the cache is an instruction cache (Malik, col. 4, lines 10-12; Fig. 3, elements 300 and 310).

Response to Arguments

26. Applicant's arguments filed December 18, 2006 with respect to **claims 1-24** have been fully considered but they are not persuasive.

27. With respect to Applicant's argument in the first paragraph on page 9 of the communication filed December 18, 2006 which states, "Applicants respectfully submit that neither Matsubara, nor Anon, nor their combination teaches or suggests "responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction" or

"responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor" as recited in claim 1" the Examiner respectfully disagrees. The Examiner refers Applicant to the rejection of claim 1 above and more specifically to Matsubara, Fig. 6B and col. 6, lines 53-55. As is clearly shown these cited sections of Matsubara, the software prefetch instruction goes through an "instruction fetch (IF)" stage during which the instruction is loaded into a cache of the processor. Responsive to the IF stage, the instruction enters the decoding stage. During the decoding stage, the bits of the instruction undergo an analysis. During this analysis the CPU (i.e. processor unit) determines whether the value of the prefetch (PF) bits is 1 or not. When the value of the PF bits is 1, it follows that a prefetch indicator is in fact associated with the instruction. Responsive to the PF bits being equal to 1 (i.e. a prefetch indicator being associated with the instruction), all the data of the line shown by an operation is prefetched to the primary cache of the CPU. As discussed in the rejection above, Anon discloses a pointer to a data structure identified by a prefetch indicator. Accordingly, the combination of Matsubara and Anon sufficiently discloses responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction, as well as, responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor.

28. With respect to Applicant's argument in the second paragraph on page 12 of the communication filed December 18, 2006, the Examiner respectfully disagrees. As

stated in the rejections above, the term 'if' denotes an optionally recited limitation and optionally recited limitations are not guaranteed to take place. Accordingly, claims 3, 13, and 20 contain language that suggests or makes optional but does not require steps to be performed or does not limit the claims to a particular structure and therefore does not limit the scope of the claims.

29. With respect to Applicant's argument in the sixth paragraph on page 12 of the communication filed December 18, 2006, the Examiner respectfully disagrees. As stated in the rejections above, the term 'if' denotes an optionally recited limitation and optionally recited limitations are not guaranteed to take place. Accordingly, claims 4, 14, and 21 contain language that suggests or makes optional but does not require steps to be performed or does not limit the claims to a particular structure and therefore does not limit the scope of the claims.

30. As for Applicant's arguments with respect to independent claims 8, 11, and 18, the arguments rely on the allegation that independent claim 1 is allowable and therefore for similar reasons independent claims 8, 11, and 18 claims are allowable. However, as addressed above, independent claim 1 is not allowable, thus, Applicant's arguments with respect to independent claims 8, 11, and 18 claims are not persuasive.

31. As for Applicant's arguments with respect to the dependent claims, the arguments rely on the allegation that independent claims 1, 8, 11, and 18 are allowable and therefore, by virtue of their dependency, the dependent claims are allowable. However, as addressed above, independent claims 1, 8, 11, and 18 are not allowable, thus, Applicant's arguments with respect to the dependent claims are not persuasive.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-24** have received a second action on the merits and are subject of a second action final.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
Art Unit 2185
March 14, 2007

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